



Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number:

0 363 882
A2

(12)

EUROPEAN PATENT APPLICATION

(21) Application number: 89118752.8

(51) Int. Cl.5: G06F 9/46

(22) Date of filing: 09.10.89

(33) Priority: 08.10.88 JP 252904/88
27.10.88 JP 269577/88
27.10.88 JP 269578/88
27.10.88 JP 269579/88
27.10.88 JP 269580/88
27.10.88 JP 269581/88

(43) Date of publication of application:
18.04.90 Bulletin 90/16

(64) Designated Contracting States:
BE DE FR GB IT NL

(71) Applicant: NEC CORPORATION
33-1, Shiba 5-chome
Minato-ku Tokyo(JP)

(72) Inventor: Hayashi, Hideo
c/o NEC Corporation 33-1, Shiba 5-chome
Minato-ku Tokyo(JP)
Inventor: Mochizuki, Atsuo
c/o NEC Koufu, Ltd. 17-14, Marunouchi
1-chome
Koufu-shi Yamanashi(JP)
Inventor: Kobayashi, Ryuji
c/o NEC Software, Ltd. 7-15, Shiba 5-chome
Minato-ku Tokyo(JP)
Inventor: Kumamoto, Chiaki
c/o NEC Software, Ltd. 7-15, Shiba 5-chome
Minato-ku Tokyo(JP)
Inventor: Kokubu, Reiko
c/o NEC Software, Ltd. 7-15, Shiba 5-chome
Minato-ku Tokyo(JP)

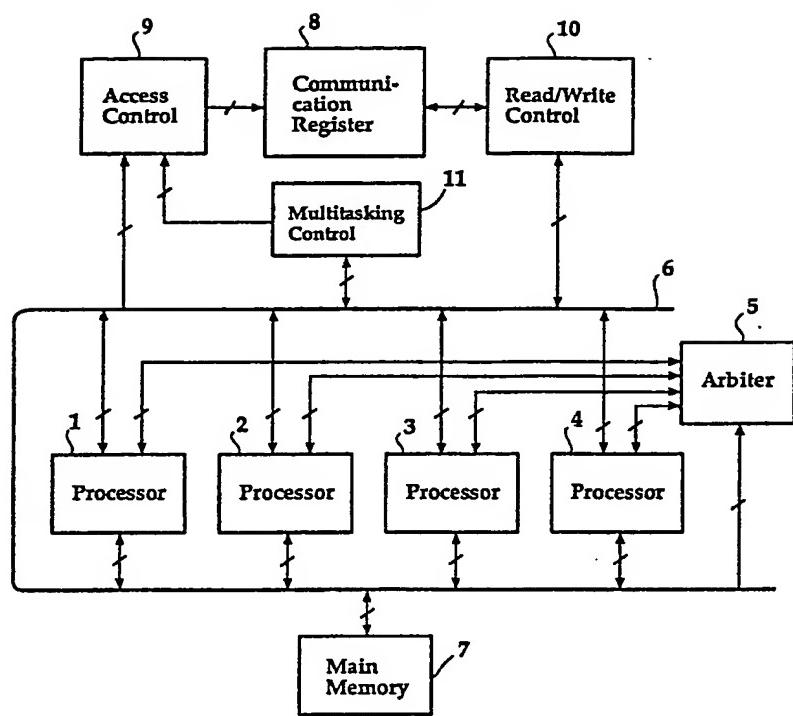
(74) Representative: Vossius & Partner
Siebertstrasse 4 P.O. Box 86 07 67
D-8000 München 86(DE)

(54) Multiprocessor system using communication register having processor-associated storage locations.

A2
882 A2
363 882
0 363 882
EP 0 363 882
Multiprocessor system using communication register having processor-associated storage locations and one of the groups is further partitioned into subgroups associated respectively with the processors. An access controller accesses any groups of the communication register when a system program is being processed and accesses one of the subgroups when a user program is being processed. A write controller is responsive to a test & set instruction of first occurrence from a common bus for assembling a lock word with a data word, a control field and a counter field containing a variable count. The control field of the lock word is set to a first binary state when it is assembled and reset to a second binary state when deassembled. In response

to a load instruction from the common bus, either the data word from the bus or lock word is stored into a specified storage area of a communication register. A read controller reads contents of an addressed location of the communication register onto the common bus in response to a save instruction. Test & set instruction of a subsequent occurrence causes the variable count in the stored lock word to be decremented as long as the control field remains set to the first binary state. When the count reduces to zero, a signal is applied to the common bus indicating the occurrence of a dead lock.

Fig. 1



Multiprocessor System Using Communication Register Having Processor-Associated Storage Locations

The present invention relates to multiprocessor systems.

The design concept of a multiprocessor system is generally to increase system throughput, but in some cases it is aimed at reducing job's turnaround time. If a job has independent tasks, the turnaround time of the job can be reduced by performing parallel processing on the whole or part of the job. In some type of parallel processing, there is a special kind of data that must be synchronized between tasks or shared by more than one processor. Such data must be used exclusively by one processor. For such purposes, a lock word is stored in a main memory. When a processor attempts to access the exclusive data, it sets the lock word if it is not set so as to obtain the right to access. Any of the other processors accessing the exclusive data examines the status of the lock word, and if it has been set already, the processor is denied access to that data until the lock word is reset. Since the lock word is stored in the main memory, there is an inherent delay in the transfer of data, thus placing a limit to the highest speed with which data can be transferred between processors. In addition to this, a dead lock condition can occur when a processor fails to reset the lock word.

It is therefore an object of the present invention to provide a multiprocessor system which allows high speed data transfer between multiple processors by writing a lock word into a communication register.

Another object of the present invention is to provide a multiprocessor system which eliminates dead lock conditions which might otherwise occur as a result of a processor failing to reset a lock word.

According to a first aspect of the present invention, a communication register is connected to a common bus, the communication register being partitioned into a plurality of groups of word storage locations. One of the groups is further partitioned into a plurality of subgroups associated respectively with the processors. An access controller accesses one of the word storage locations of all groups of the communication register in accordance with a first address code of longer bit length supplied from the common bus when the granted processor is processing a system program and for accessing a storage location of one of the subgroups in accordance with a second address code of shorter bit length supplied from the common bus and contents of directories which are associated respectively with the processors when

the granted processor is processing a user program. A write controller writes a data word of longer bit length from the common bus into a word storage location of the communication register specified by the access controller and forms a lock word with a data word of shorter bit length from the common bus and writes the lock word into a specified word storage location of the communication register. A read controller reads out contents of a storage location of the communication register specified by the access controller and forwards them onto the common bus.

According to a second aspect, the access controller accesses a specified storage area of the communication register in accordance with an address code supplied from the common bus. A write controller is responsive to a test & set instruction of first occurrence from the common bus for assembling a lock word with an exclusive data word supplied from the common bus, a control field and a counter field containing a variable count. The control field of the lock word is set to a first binary state when the lock word is assembled and reset to a second binary state when the lock word is deassembled. The write controller is further responsive to a load instruction from the common bus for writing a non-exclusive data word received from the bus as well as the lock word into a storage area of the communication register specified by the address controller. In response to a save instruction, a read controller reads a word out of the communication register onto the common bus. Responsive to the test & set instruction of a subsequent occurrence from the common bus, the count value in the stored lock word is varied by a predetermined amount as long as the control field remains set to the first binary state. A detector is provided to apply a signal to the common bus indicating the occurrence of an abnormal condition when the count value attains a predetermined value.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be described in further detail with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram of a multiprocessor system according to the present invention;

Fig. 2A is a block diagram of the communication register and the address controller of Fig. 1;

Fig. 2B is a block diagram of the commu-

nication register and the read/write controller of Fig. 1;

Fig. 3 shows formats of data stored in the communication register of Fig. 2A;

Fig. 4 shows a format of data stored in a directory control register of the multitasking controller of Fig. 2A;

Figs. 5A and 5B are flowcharts describing a sequence of operations performed by the multitasking controller; and

Fig. 6 is a schematic illustration of the contents of communication register directories used in a multitasking environment.

DETAILED DESCRIPTION

Referring now to Fig. 1, there is shown a multiprocessor system according to an embodiment of the present invention. Four processors 1, 2 3 and 4 are provided. A bus arbiter 5 receives a request from the processors when they attempt to access a common bus 6. Permission is granted to only one processor if there is more than one competing processor. Through the common bus 6 each processor communicates with a main memory 7 and a communication register 8 for exchanging data with other processors. An access controller 9 and a read/write controller 10 are connected to the common bus 6 to access the communication register 8 and write data from a granted processor into a specified word location of the communication register 8 and read it from a specified area of the register. 8. A multitasking controller 11 is further connected between bus 6 and access controller 9 to permit multitasking operations to be performed between the processors in a master-slave relationship.

As illustrated in Fig. 2A, the communication register 8 is partitioned into 256 words of 64 bits each. The register 8 is divided into a group A of #0 to #127 words and a group B of #128 to #255 words. Group B of the register 8 is further divided into subgroups B1 (#128 to #159), B2 (#160 to #191), B3 (#192 to #223) and B4 (#224 to #255).

Access controller 9 comprises a processor identifier register 20, a mode register 21 and a 64-bit address register 22, all of which are connected to the common bus 6 to receive and store data supplied from a processor to which permission is granted from the bus arbiter 5. The identifier number of the accessing processor is stored in the processor identifier register 20, and a mode identifier bit of the processor is stored in the mode register 21. When the processor is performing a system program, it is said to be in a high-priority mode and a logical 1 is stored in the mode register

21 and when performing a user program it is said to be in a low-priority mode and a logical 0 is stored in the register 21. Mode register 21 has output leads 21a and 21b which are connected to adders 29 and 30, respectively. During the high-priority mode, the mode register outputs at leads 21a and 21b are logical 1 and 0, respectively, and during the low-priority mode, the logical levels at leads 21a and 21b are at 0 and 1, respectively.

To permit full access to the whole area of communication register 8 when the system program is being executed, an 8-bit address data is stored in the #56 to #63 bit positions of the 64-bit address register 22 which are connected to adder 29. The output of adder 29 is supplied to the communication register 8 to access a desired word location from any of the 256 word locations of the communication register 8.

Partial access to the register 8 is given to a processor when executing a user program. In this case, a 5-bit address code is stored in the #59 to #63 bit positions of the address register 22 to identify any one of 32 word locations of a subgroup which is addressed. These bit positions are connected to an adder 30 to which the output lead 21b of mode register 21 is also connected. The output of processor identifier register 20 is translated by a decoder 23 into a 4-bit code which is supplied to comparators 24, 25, 26 and 27 for comparison with 4-bit codes supplied respectively from communication register directories 31, 32, 33 and 34 which are, in turn, associated with subgroups B1, B2, B3 and B4 of the communication register 8, respectively.

Each of the directories 31, 32, 33 and 34 has four bit positions. Normally, a logical 1 is set into the first (leftmost) bit position of directory 31, the second bit position of directory 32, the third bit position of directory 33 and the fourth (rightmost) bit position of directory 34 as illustrated in Fig. 2A. The bit position of each directory in which a logical 1 is stored identifies the processor with which the directory is associated, so that directories 31, 32, 33 and 34 are normally associated with processors 1, 2, 3 and 4, respectively. Since directories 31 to 34 are associated with subgroups B1 to B4, respectively, processors 1 to 4 are normally associated with subgroups B1 to B4, respectively.

Each of the comparators 24 to 27 produces a logical-1 output when there is a match between the input from the decoder 23 and the input from the associated directory and produces a logical 0 output when there is no match between them. A 4-bit code is thus formed by the outputs of comparators 24 to 27 and translated by an encoder 28 into a 2-bit subgroup identifying code, which is applied to the adder 30 and appended with the 5-bit word identifying code to access any location of a speci-

fied one of subgroups B1 through B4. To the leftmost position of the 5-bit code is appended a logical 1 which is supplied from the mode register 21 during a low-priority mode. With a word location of the communication register 8 being identified by the access controller 9, a 64-bit word can be exchanged between the processor and the communication register 8 and this operation is handled by the read/write controller 10 of Fig. 2B.

Read/write controller 10 includes an instruction register 40 and a 64-bit input data register 41 both of which are connected to the bus 6. Instruction register 40 receives three types of instruction from the processors, which are SAVE, LOAD and TEST & SET instructions. Input data register 41 receives a 64-bit data word of a 32-bit "exclusive" data word from the bus 6. An output data register 46 is connected to the communication register 8 to store a data word or a lock word and transfers them to the bus 6 in response to an output from an OR gate 47 to which SAVE and TEST & SET instructions are supplied from a decoder 42.

Data stored in the instruction register 40 is examined by decoder 42 to selectively control the data stored in the input data register 41, depending on whether the instruction is LOAD or TEST & SET as well as on the logical state of the #0 bit position of the output data register 46.

The #0 bit position of the output data register 46 is connected to a zero detector 49 as well as to an AND gate 43 and an inverter 44, and further to the #0 bit position of the input of communication register 8. The #8 to #31 bit positions of the output data register 46 are connected to a decrement circuit 48 whose outputs are connected to the #8 to #31 bit positions of the input of communication register 8 as well as to the zero detector 49. The #32 to #63 bit positions of the output data register 46 are connected to the corresponding bit positions of communication register 8.

Each of the 64-bit words stored in the communication register 8 may be of a 64-bit length data word format as shown in part (a) of Fig. 3, or of a lock word format as shown in part (b) of Fig. 3. In the former case, the communication register 8 is used as a data register and in the latter case, the data word is partitioned into a lock/unlock bit position (#0), a 24-bit counter field (#8 to #31 bit positions) and a 32-bit data field (#32 to #63 bit positions). The lock/unlock bit is set to logical 1 when exclusive control is being carried out and is reset to logical 0 when exclusive control is released.

If the input data is a 64-bit data word, it is supplied to the communication register 8 and if it is a 32-bit "exclusive" data word, a lock/unlock bit and a counter field are appended to it to form a lock word. In response to a LOAD instruction the

contents of the input data register 41 are loaded into a word location of the communication register 8 which is specified by the access controller 9 in a manner as described previously.

If a logical 0 is reset in the #0 bit position of a lock word, a logical 0 appears in the #0 bit position of the output data register 46. A TEST & SET instruction causes the output data register 46 to read the stored lock word, so that AND gate 45 is activated to set a logical 1 into the #0 position of the input of communication register 8, and set all 1's into the #8 to #31 bit positions of the register 8 input. In this instance, the #32 to #63 bit input positions are filled with data bits of a 32-bit "exclusive" data word. In this way, a new lock word is assembled with a counter field set with a maximum count value. In response to a TEST & SET instruction, this lock word is stored into a specified location of the communication register 8. The processor, which has issued this TEST & SET instruction, receives this lock word and checks its #0 bit position in response to receipt of a subsequent command to see whether the attempt to set a lock word has been successful or failed. If the attempt has failed, the processor generates a TEST & SET instruction again to repeat the above process until the stored lock word is reset by another processor which has set it previously.

With a logical 1 being set in the #0 bit position of a lock word, a logical 1 appears in the #0 bit position of output data register 46. A subsequent TEST & SET instruction from a processor causes the output data register 46 to read a stored lock word from register 8 and deactivates AND gate 45 and activates AND gate 43. As a result, the count value set in the counter field (#8 to #31 bit positions) of the lock word is decremented by one in the decrement circuit 48, and communication register 8 receives the outputs of decrement circuit 48 and an "exclusive" data word from the #32 to #63 bit positions of output data register 46. The contents of the output data register 46 are therefore updated and stored again into the communication register 8. It is seen therefore that the value set in the counter field of a lock word is reduced to zero when it has been decremented 2^{24} times from the initial value each time the communication register 8 is accessed with a TEST & SET instruction.

In response to a SAVE instruction, the output data register 46 transfers the contents of the output data register 46 to the bus 6.

Zero detector 49 is enabled in response to the output of AND gate 43 to supply a signal to the bus 6 indicating the occurrence of a deadlock condition when the logical value decremented by the decrement circuit 48 is reduced to zero. When this occurs, the processor of interest enters a subroutine to remove the deadlock condition.

The contents of communication register directories 31 through 34 are controlled by a 64-bit directory control instruction supplied from a processor to a directory control register contained in the multitasking controller 11 as shown in Fig. 4. The directory control instruction data includes a control bit in the #55 bit position and master processor identifiers in the #60 to #63 bit positions associated respectively with processors 1, 2, 3 and 4. A logical 1 in the #60 to #63 bit positions of the directory control data indicates that a master processor is one that is associated with that bit location. As shown in Figs. 5A and 5B, multitasking controller 11 is programmed to perform directories set and reset operations.

In Fig. 5A, the program starts with decision block 50 which examines the control bit (C) to check to see if it is logical 1 or 0. If C=1, exit is to decision block 51 to determine which one of the processors has been granted access to the communication register 8. Depending on the identified processor number, control exits to one of operations blocks 52 to 55 to reset a bit position of a respective one of the directories 31 to 34. Following blocks 52 to 55, exit is to one of blocks 56 to 59 associated respectively with blocks 52 to 55 to set a variable n with a processor identifier detected by block 51. Control then exits to decision block 60 to detect which one of the #60 to #63 bit positions of the directory control data is set with a logical 1. Depending on the decision made by block 60, control proceeds to one of operations blocks 61 to 64 to set the #n bit position of a respective one of the directories.

If, for example, processor 3 acts as a slave processor performing a multitasking operation with processor 2 which acts as a master processor, the control bit of a directory set instruction from processor 3 is set to 1 as shown in Fig. 6, and control exits from block 51 to block 54 to reset the #3 bit position of directory 33 to 0 as indicated by a dotted line 33a in Fig. 6. Control advances to block 58 to set n to 3. Since processor 2 is the master processor, a 1 is set in the #61 bit position of the directory control data and control exits to block 62 to set a 1 into #2 bit position of directory 32 as indicated by a dotted line 32a. In this way, the #2 and #3 bit positions of directory 32 are set with a logical 1. The contents of these bit positions are accessed by processors 2 and 3 to perform a multitasking operation.

When resetting the contents of directory 32, a directory reset instruction containing C=0 is supplied from processor 3 to the directory control register of multitasking controller 11 as shown in Fig. 6. In Fig. 5A, the program starts with decision block 65 after checking that C=0. Exit then is to decision block 66 (Fig. 5B) to determine whether

the variable n is 1,2,3 or 4. Depending on the variable n, control exits to one of operations blocks 67 to 70 to set a bit position of a respective one of the directories 31 to 34. Following blocks 67 to 70, exit is to decision block 71 to detect which one of the #60 to #63 bit positions of the directory reset instruction is set with a logical 1. Depending on the decision made by block 60, control proceeds to one of operations blocks 72 to 75 to reset the #n bit position of a respective one of the directories.

Therefore, in response to the directory reset instruction from processor 3, control exits from block 66 to block 68 to set the #3 bit position of directory 33 to 1 as indicated by a dotted line 33b. Control advances to block 73 to reset #2 bit position of directory 32 to 0 as indicated by a dotted line 32b. In this way, directories 32 and 33 are reset to normal to terminate the multitasking operation.

The foregoing description shows only one preferred embodiment of the present invention. Various modifications are apparent to those skilled in the art without departing from the scope of the present invention which is only limited by the appended claims. Therefore, the embodiment shown and described is only illustrative, not restrictive.

Claims

- 30 1. A multiprocessor system having a plurality of processors connected to a common bus, means for granting permission to one of said processors to access said common bus, and a main memory connected to said common bus for storing data to be exchanged between said processors, comprising:
a communication register connected to said common bus, said communication register being partitioned into a plurality of groups of word storage locations, one of said groups being further partitioned into a plurality of subgroups associated respectively with said processors;
first access control means for accessing one of the word storage locations of said first and second groups of said communication register in accordance with a first address code of longer bit length supplied from said common bus when the granted processor is operating in a first mode;
- 35 2. A plurality of directories associated respectively with said subgroups, each of said directories having a plurality of bit positions associated respectively with said processors;
- 40 3. Second access control means for accessing one of the word storage locations of one of said subgroups in accordance with a second address code of shorter bit length supplied from said common bus and contents of the bit positions of said direc-
- 45
- 50
- 55

tories when the granted processor is operating in a second mode;

write control means for writing a data word of longer bit length from said common bus into a word storage location of the communication register either specified by the first or second access control means, forming a lock word with a data word of shorter bit length from said bus and writing the lock word into the specified word storage location of the communication register; and
read control means for reading contents of a word storage location of said communication register specified by either of said first and second access control means onto said common bus.

2. A multiprocessor system as claimed in claim 1, further comprising multitasking control means for rewriting the contents of said directories in accordance with a directory control instruction from said granted processor when same is performing a multitasking operation with a master processor indicated by said directory control information.

3. A multiprocessor system as claimed in claim 2, wherein said directories are organized into a matrix of rows and columns, both of said rows and columns being respectively associated with said processors, the intersections of said rows and columns corresponding to the bit positions of said directories, wherein said multitasking control means rewrites the bit position of a directory at the intersection of the row and column which are associated with the granted processor, and rewrites the bit position of a directory at the intersection of the row which is associated with said master processor and the column which is associated with said granted processor.

4. A multiprocessor system as claimed in any one of claims 1 to 3, wherein said write control means is responsive to a test & set instruction of first occurrence from said common bus for assembling said lock word with said data word of shorter bit length, a control field and a counter field containing a variable count, said control field being set to a first binary state when said lock word is assembled and reset to a second binary state when said lock word is deassembled, said write control means being further responsive to a load instruction from said common bus for writing said lock word into a word storage area of said communication register specified by either of said first and second address control means;

means responsive to the test & set instruction of a subsequent occurrence from said common bus for varying said variable count in the stored lock word by a predetermined amount when said control field remains set to said first binary state; and

means for applying a signal to said common bus indicating the occurrence of an abnormal condition when said variable count attains a predetermined

value.

5. A multiprocessor system as claimed in any one of claims 1 to 4, wherein said write control means comprises:

- 5 input means connected to said common bus for receiving said data words of longer or shorter bit length; and
a logic circuit responsive to said test & set instruction for storing a predetermined bit into a first bit position of said input means and all 1's into second bit positions of the input means, and responsive to said load instruction for loading the contents of said input means into a specified storage word location of said communication register, said input means containing said data word in third bit positions thereof, wherein said read control means comprises:
- 10 output means connected to said communication register for receiving contents of a specified word storage location of said communication register in response to each of said test & set instruction and said save instruction, said output means having a first bit position connected to the first bit position of said input means, second bit positions connected to said varying means and third bit positions connected to the third bit positions of said input means, all bit positions of said output means being connected to said common bus,
- 15 said logical circuit being responsive to the predetermined bit in said first bit position of said output means for rewriting the second bit positions of said input means with outputs of said varying means and rewriting the third bit positions of said input means with contents of the third bit positions of said output means.

- 20 30 35 40 45 50 55 60 65 70 75 80 85 90 95 100 105 110 115 120 125 130 135 140 145 150 155 160 165 170 175 180 185 190 195 200 205 210 215 220 225 230 235 240 245 250 255 260 265 270 275 280 285 290 295 300 305 310 315 320 325 330 335 340 345 350 355 360 365 370 375 380 385 390 395 400 405 410 415 420 425 430 435 440 445 450 455 460 465 470 475 480 485 490 495 500 505 510 515 520 525 530 535 540 545 550 555 560 565 570 575 580 585 590 595 600 605 610 615 620 625 630 635 640 645 650 655 660 665 670 675 680 685 690 695 700 705 710 715 720 725 730 735 740 745 750 755 760 765 770 775 780 785 790 795 800 805 810 815 820 825 830 835 840 845 850 855 860 865 870 875 880 885 890 895 900 905 910 915 920 925 930 935 940 945 950 955 960 965 970 975 980 985 990 995 1000 1005 1010 1015 1020 1025 1030 1035 1040 1045 1050 1055 1060 1065 1070 1075 1080 1085 1090 1095 1100 1105 1110 1115 1120 1125 1130 1135 1140 1145 1150 1155 1160 1165 1170 1175 1180 1185 1190 1195 1200 1205 1210 1215 1220 1225 1230 1235 1240 1245 1250 1255 1260 1265 1270 1275 1280 1285 1290 1295 1300 1305 1310 1315 1320 1325 1330 1335 1340 1345 1350 1355 1360 1365 1370 1375 1380 1385 1390 1395 1400 1405 1410 1415 1420 1425 1430 1435 1440 1445 1450 1455 1460 1465 1470 1475 1480 1485 1490 1495 1500 1505 1510 1515 1520 1525 1530 1535 1540 1545 1550 1555 1560 1565 1570 1575 1580 1585 1590 1595 1600 1605 1610 1615 1620 1625 1630 1635 1640 1645 1650 1655 1660 1665 1670 1675 1680 1685 1690 1695 1700 1705 1710 1715 1720 1725 1730 1735 1740 1745 1750 1755 1760 1765 1770 1775 1780 1785 1790 1795 1800 1805 1810 1815 1820 1825 1830 1835 1840 1845 1850 1855 1860 1865 1870 1875 1880 1885 1890 1895 1900 1905 1910 1915 1920 1925 1930 1935 1940 1945 1950 1955 1960 1965 1970 1975 1980 1985 1990 1995 2000 2005 2010 2015 2020 2025 2030 2035 2040 2045 2050 2055 2060 2065 2070 2075 2080 2085 2090 2095 2100 2105 2110 2115 2120 2125 2130 2135 2140 2145 2150 2155 2160 2165 2170 2175 2180 2185 2190 2195 2200 2205 2210 2215 2220 2225 2230 2235 2240 2245 2250 2255 2260 2265 2270 2275 2280 2285 2290 2295 2300 2305 2310 2315 2320 2325 2330 2335 2340 2345 2350 2355 2360 2365 2370 2375 2380 2385 2390 2395 2400 2405 2410 2415 2420 2425 2430 2435 2440 2445 2450 2455 2460 2465 2470 2475 2480 2485 2490 2495 2500 2505 2510 2515 2520 2525 2530 2535 2540 2545 2550 2555 2560 2565 2570 2575 2580 2585 2590 2595 2600 2605 2610 2615 2620 2625 2630 2635 2640 2645 2650 2655 2660 2665 2670 2675 2680 2685 2690 2695 2700 2705 2710 2715 2720 2725 2730 2735 2740 2745 2750 2755 2760 2765 2770 2775 2780 2785 2790 2795 2800 2805 2810 2815 2820 2825 2830 2835 2840 2845 2850 2855 2860 2865 2870 2875 2880 2885 2890 2895 2900 2905 2910 2915 2920 2925 2930 2935 2940 2945 2950 2955 2960 2965 2970 2975 2980 2985 2990 2995 3000 3005 3010 3015 3020 3025 3030 3035 3040 3045 3050 3055 3060 3065 3070 3075 3080 3085 3090 3095 3100 3105 3110 3115 3120 3125 3130 3135 3140 3145 3150 3155 3160 3165 3170 3175 3180 3185 3190 3195 3200 3205 3210 3215 3220 3225 3230 3235 3240 3245 3250 3255 3260 3265 3270 3275 3280 3285 3290 3295 3300 3305 3310 3315 3320 3325 3330 3335 3340 3345 3350 3355 3360 3365 3370 3375 3380 3385 3390 3395 3400 3405 3410 3415 3420 3425 3430 3435 3440 3445 3450 3455 3460 3465 3470 3475 3480 3485 3490 3495 3500 3505 3510 3515 3520 3525 3530 3535 3540 3545 3550 3555 3560 3565 3570 3575 3580 3585 3590 3595 3600 3605 3610 3615 3620 3625 3630 3635 3640 3645 3650 3655 3660 3665 3670 3675 3680 3685 3690 3695 3700 3705 3710 3715 3720 3725 3730 3735 3740 3745 3750 3755 3760 3765 3770 3775 3780 3785 3790 3795 3800 3805 3810 3815 3820 3825 3830 3835 3840 3845 3850 3855 3860 3865 3870 3875 3880 3885 3890 3895 3900 3905 3910 3915 3920 3925 3930 3935 3940 3945 3950 3955 3960 3965 3970 3975 3980 3985 3990 3995 4000 4005 4010 4015 4020 4025 4030 4035 4040 4045 4050 4055 4060 4065 4070 4075 4080 4085 4090 4095 4100 4105 4110 4115 4120 4125 4130 4135 4140 4145 4150 4155 4160 4165 4170 4175 4180 4185 4190 4195 4200 4205 4210 4215 4220 4225 4230 4235 4240 4245 4250 4255 4260 4265 4270 4275 4280 4285 4290 4295 4300 4305 4310 4315 4320 4325 4330 4335 4340 4345 4350 4355 4360 4365 4370 4375 4380 4385 4390 4395 4400 4405 4410 4415 4420 4425 4430 4435 4440 4445 4450 4455 4460 4465 4470 4475 4480 4485 4490 4495 4500 4505 4510 4515 4520 4525 4530 4535 4540 4545 4550 4555 4560 4565 4570 4575 4580 4585 4590 4595 4600 4605 4610 4615 4620 4625 4630 4635 4640 4645 4650 4655 4660 4665 4670 4675 4680 4685 4690 4695 4700 4705 4710 4715 4720 4725 4730 4735 4740 4745 4750 4755 4760 4765 4770 4775 4780 4785 4790 4795 4800 4805 4810 4815 4820 4825 4830 4835 4840 4845 4850 4855 4860 4865 4870 4875 4880 4885 4890 4895 4900 4905 4910 4915 4920 4925 4930 4935 4940 4945 4950 4955 4960 4965 4970 4975 4980 4985 4990 4995 5000 5005 5010 5015 5020 5025 5030 5035 5040 5045 5050 5055 5060 5065 5070 5075 5080 5085 5090 5095 5100 5105 5110 5115 5120 5125 5130 5135 5140 5145 5150 5155 5160 5165 5170 5175 5180 5185 5190 5195 5200 5205 5210 5215 5220 5225 5230 5235 5240 5245 5250 5255 5260 5265 5270 5275 5280 5285 5290 5295 5300 5305 5310 5315 5320 5325 5330 5335 5340 5345 5350 5355 5360 5365 5370 5375 5380 5385 5390 5395 5400 5405 5410 5415 5420 5425 5430 5435 5440 5445 5450 5455 5460 5465 5470 5475 5480 5485 5490 5495 5500 5505 5510 5515 5520 5525 5530 5535 5540 5545 5550 5555 5560 5565 5570 5575 5580 5585 5590 5595 5600 5605 5610 5615 5620 5625 5630 5635 5640 5645 5650 5655 5660 5665 5670 5675 5680 5685 5690 5695 5700 5705 5710 5715 5720 5725 5730 5735 5740 5745 5750 5755 5760 5765 5770 5775 5780 5785 5790 5795 5800 5805 5810 5815 5820 5825 5830 5835 5840 5845 5850 5855 5860 5865 5870 5875 5880 5885 5890 5895 5900 5905 5910 5915 5920 5925 5930 5935 5940 5945 5950 5955 5960 5965 5970 5975 5980 5985 5990 5995 6000 6005 6010 6015 6020 6025 6030 6035 6040 6045 6050 6055 6060 6065 6070 6075 6080 6085 6090 6095 6100 6105 6110 6115 6120 6125 6130 6135 6140 6145 6150 6155 6160 6165 6170 6175 6180 6185 6190 6195 6200 6205 6210 6215 6220 6225 6230 6235 6240 6245 6250 6255 6260 6265 6270 6275 6280 6285 6290 6295 6300 6305 6310 6315 6320 6325 6330 6335 6340 6345 6350 6355 6360 6365 6370 6375 6380 6385 6390 6395 6400 6405 6410 6415 6420 6425 6430 6435 6440 6445 6450 6455 6460 6465 6470 6475 6480 6485 6490 6495 6500 6505 6510 6515 6520 6525 6530 6535 6540 6545 6550 6555 6560 6565 6570 6575 6580 6585 6590 6595 6600 6605 6610 6615 6620 6625 6630 6635 6640 6645 6650 6655 6660 6665 6670 6675 6680 6685 6690 6695 6700 6705 6710 6715 6720 6725 6730 6735 6740 6745 6750 6755 6760 6765 6770 6775 6780 6785 6790 6795 6800 6805 6810 6815 6820 6825 6830 6835 6840 6845 6850 6855 6860 6865 6870 6875 6880 6885 6890 6895 6900 6905 6910 6915 6920 6925 6930 6935 6940 6945 6950 6955 6960 6965 6970 6975 6980 6985 6990 6995 7000 7005 7010 7015 7020 7025 7030 7035 7040 7045 7050 7055 7060 7065 7070 7075 7080 7085 7090 7095 7100 7105 7110 7115 7120 7125 7130 7135 7140 7145 7150 7155 7160 7165 7170 7175 7180 7185 7190 7195 7200 7205 7210 7215 7220 7225 7230 7235 7240 7245 7250 7255 7260 7265 7270 7275 7280 7285 7290 7295 7300 7305 7310 7315 7320 7325 7330 7335 7340 7345 7350 7355 7360 7365 7370 7375 7380 7385 7390 7395 7400 7405 7410 7415 7420 7425 7430 7435 7440 7445 7450 7455 7460 7465 7470 7475 7480 7485 7490 7495 7500 7505 7510 7515 7520 7525 7530 7535 7540 7545 7550 7555 7560 7565 7570 7575 7580 7585 7590 7595 7600 7605 7610 7615 7620 7625 7630 7635 7640 7645 7650 7655 7660 7665 7670 7675 7680 7685 7690 7695 7700 7705 7710 7715 7720 7725 7730 7735 7740 7745 7750 7755 7760 7765 7770 7775 7780 7785 7790 7795 7800 7805 7810 7815 7820 7825 7830 7835 7840 7845 7850 7855 7860 7865 7870 7875 7880 7885 7890 7895 7900 7905 7910 7915 7920 7925 7930 7935 7940 7945 7950 7955 7960 7965 7970 7975 7980 7985 7990 7995 8000 8005 8010 8015 8020 8025 8030 8035 8040 8045 8050 8055 8060 8065 8070 8075 8080 8085 8090 8095 8100 8105 8110 8115 8120 8125 8130 8135 8140 8145 8150 8155 8160 8165 8170 8175 8180 8185 8190 8195 8200 8205 8210 8215 8220 8225 8230 8235 8240 8245 8250 8255 8260 8265 8270 8275 8280 8285 8290 8295 8300 8305 8310 8315 8320 8325 8330 8335 8340 8345 8350 8355 8360 8365 8370 8375 8380 8385 8390 8395 8400 8405 8410 8415 8420 8425 8430 8435 8440 8445 8450 8455 8460 8465 8470 8475 8480 8485 8490 8495 8500 8505 8510 8515 8520 8525 8530 8535 8540 8545 8550 8555 8560 8565 8570 8575 8580 8585 8590 8595 8600 8605 8610 8615 8620 8625 8630 8635 8640 8645 8650 8655 8660 8665 8670 8675 8680 8685 8690 8695 8700 8705 8710 8715 8720 8725 8730 8735 8740 8745 8750 8755 8760 8765 8770 8775 8780 8785 8790 8795 8800 8805 8810 8815 8820 8825 8830 8835 8840 8845 8850 8855 8860 8865 8870 8875 8880 8885 8890 8895 8900 8905 8910 8915 8920 8925 8930 8935 8940 8945 8950 8955 8960 8965 8970 8975 8980 8985 8990 8995 9000 9005 9010 9015 9020 9025 9030 9035 9040 9045 9050 9055 9060 9065 9070 9075 9080 9085 9090 9095 9100 9105 9110 9115 9120 9125 9130 9135 9140 9145 9150 9155 9160 9165 9170 9175 9180 9185 9190 9195 9200 9205 9210 9215 9220 9225 9230 9235 9240 9245 9250 9255 9260 9265 9270 9275 9280 9285 9290 9295 9300 9305 9310 9315 9320 9325 9330 9335 9340 9345 9350 9355 9360 9365 9370 9375 9380 9385 9390 9395 9400 9405 9410 9415 9420 9425 9430 9435 9440 9445 9450 9455 9460 9465 9470 9475 9480 9485 9490 9495 9500 9505 9510 9515 9520 9525 9530 9535 9540 9545 9550 9555 9560 9565 9570 9575 9580 9585 9590 9595 9600 9605 9610 9615 9620 9625 9630 9635 9640 9645 9650 9655 9660 9665 9670 9675 9680 9685 9690 9695 9700 9705 9710 9715 9720 9725 9730 9735 9740 9745 9750 9755 9760 9765 9770 9775 9780 9785 9790 9795 9800 9805 9810 9815 9820 9825 9830 9835 9840 9845 9850 9855 9860 9865 9870 9875 9880 9885 9890 9895 9900 9905 9910 9915 9920 9925 9930 9935 9940 9945 9950 9955 9960 9965 9970 9975 9980 9985 9990 9995 9999 10000 10005 10010 10015 10020 10025 10030 10035 10040 10045 10050 10055 10060 10065 10070 10075 10080 10085 10090 10095 10100 10105 10110 10115 10120 10125 10130 10135 10140 10145 10150 10155 10160 10165 10170 10175 10180 10185 10190 10195 10200 10205 10210 10215 10220 10225 10230 10235 10240 10245 10250 10255 10260 10265 10270 10275 1

common bus for writing a non-exclusive data word from said bus and said lock word into a storage area of said communication register specified by said address control means;

read control means for reading a word from said communication register onto said common bus in response to a save instruction therefrom;

means responsive to the test & set instruction of a subsequent occurrence from said common bus for varying said variable count in the stored lock word by a predetermined amount when said control field remains set to said first binary state; and

means for applying a signal to said common bus indicating the occurrence of an abnormal condition when said variable count attains a predetermined value.

7. A multiprocessor system as claimed in claim 6, wherein said communication register is partitioned into first and second groups of equal size and said second group is further partitioned into a plurality of equal subgroups respectively associated with said processors, wherein said processors operate in one of first and second modes, wherein said access control means accesses any of said first and second groups when the granted processor is operating in said first mode and accesses one of said subgroups which is associated with said granted processor when same is operating in said second mode.

8. A multiprocessor system as claimed in claim 7, wherein said access control means further comprises:

a plurality of directories associated respectively with said subgroups, each of said directories having a plurality of bit positions associated respectively with said processors; and

means for addressing one of said subgroups in accordance with an address code supplied from said granted processor and contents of the bit positions of said directories when the granted processor is operating in said second mode.

9. A multiprocessor system as claimed in claim 8, further comprising multitasking control means for rewriting the contents of said directories in accordance with a directory control instruction from said granted processor when same is performing a multitasking operation with a master processor indicated by said directory control information.

10. A multiprocessor system as claimed in claim 9, wherein said directories are organized into a matrix of rows and columns, both of said rows and columns being respectively associated with said processors, the intersections of said rows and columns corresponding to the bit positions of said directories, wherein said multitasking control means rewrites the bit position of a directory at the intersection of the row and column which are associated with the granted processor, and rewrites the

bit position of a directory at the intersection of the row which is associated with said master processor and the column which is associated with said granted processor.

5 11. A multiprocessor system as claimed in any one of claims 6 to 10, wherein said write control means comprises:

input means connected to said common bus and said communication register; and

10 a logic circuit responsive to said test & set instruction for storing a predetermined bit into a first bit position of said input means and all 1's into second bit positions of the input means, and responsive to said load instruction for loading the contents of said

15 input means into a specified area of said communication register, said input means storing said exclusive data word in third bit positions thereof, wherein said read control means comprises:

output means connected to said communication register for receiving contents of a specified area of said communication register in response to either of said test & set instruction or said save instruction, said output means having a first bit position connected to the first bit position of said input means, second bit positions connected to said varying means and third bit positions connected to the third bit positions of said input means, all bit positions of said output means being connected to said common bus,

20 30 said logical circuit being responsive to the predetermined bit in said first bit position of said output means for rewriting the second bit positions of said input means with outputs of said varying means and rewriting the third bit positions of said input means with contents of the third bit positions of said output means.

25

35

40

45

50

55

Fig. 1

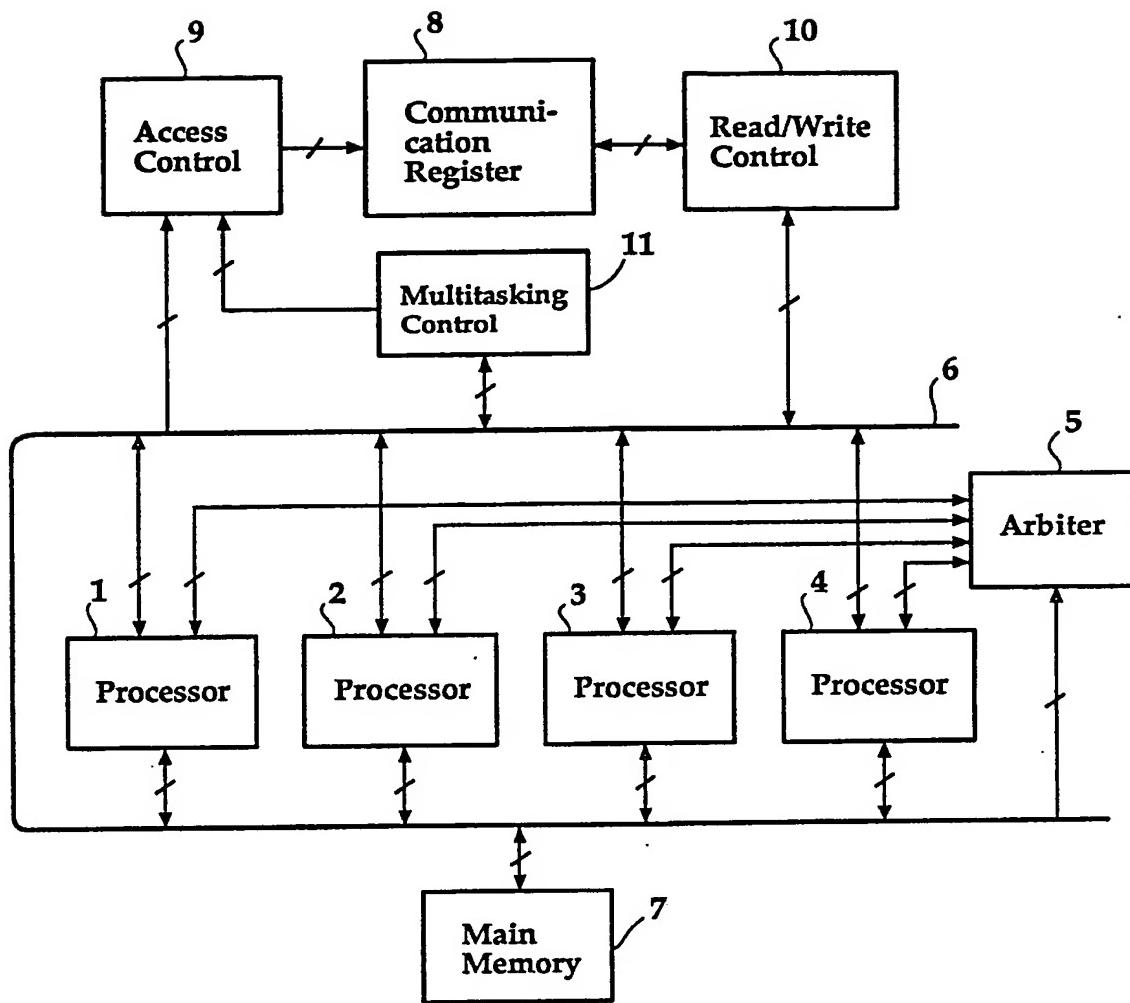


Fig. 3

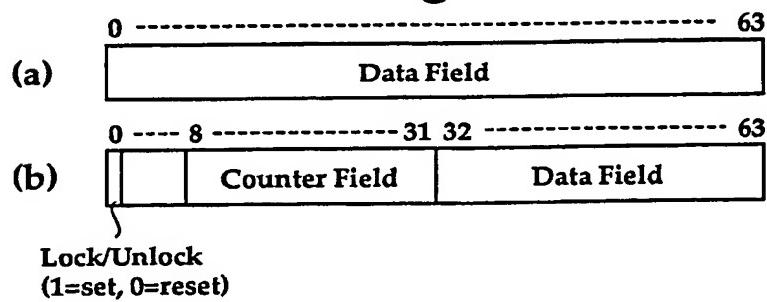
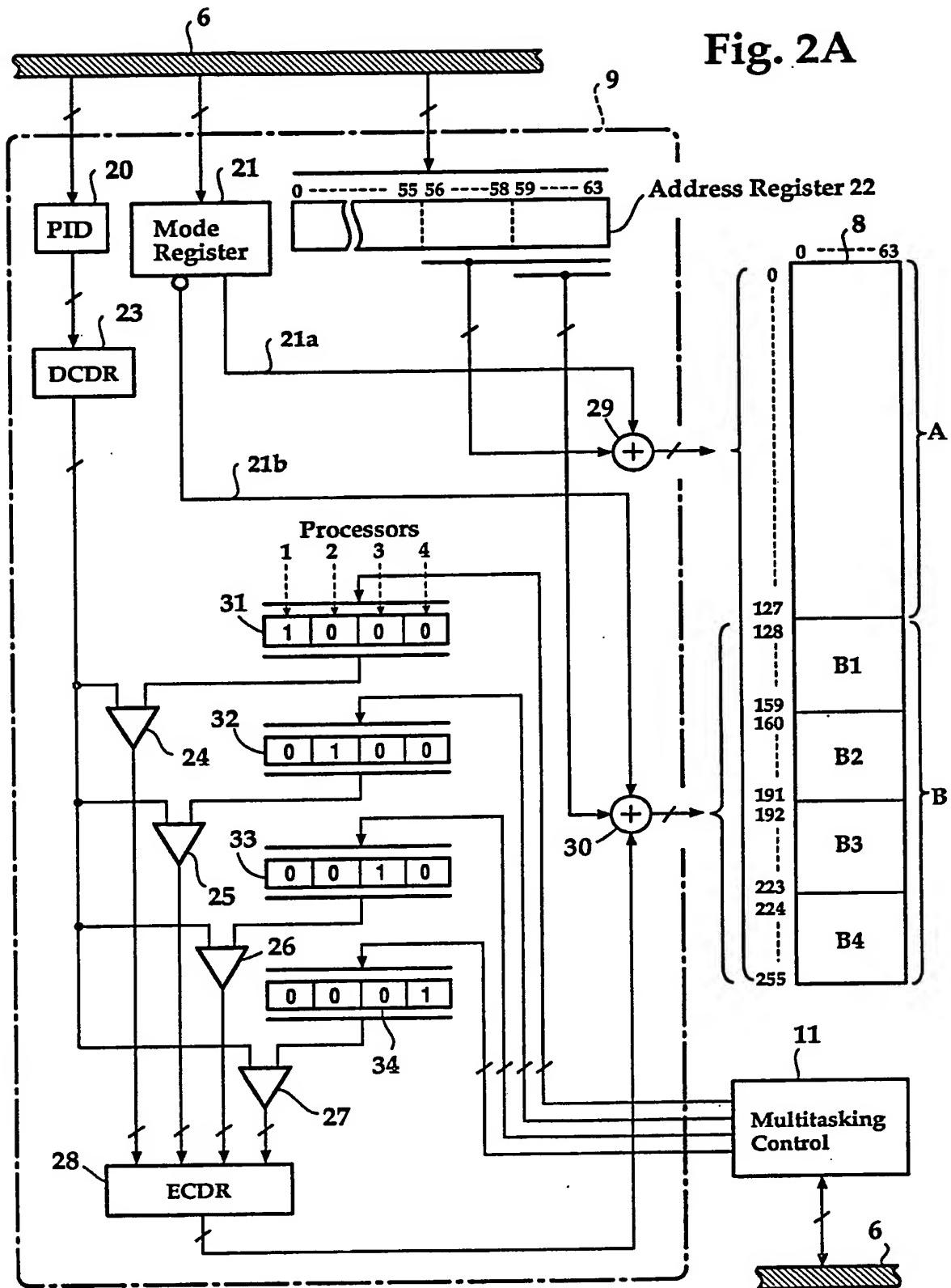


Fig. 2A



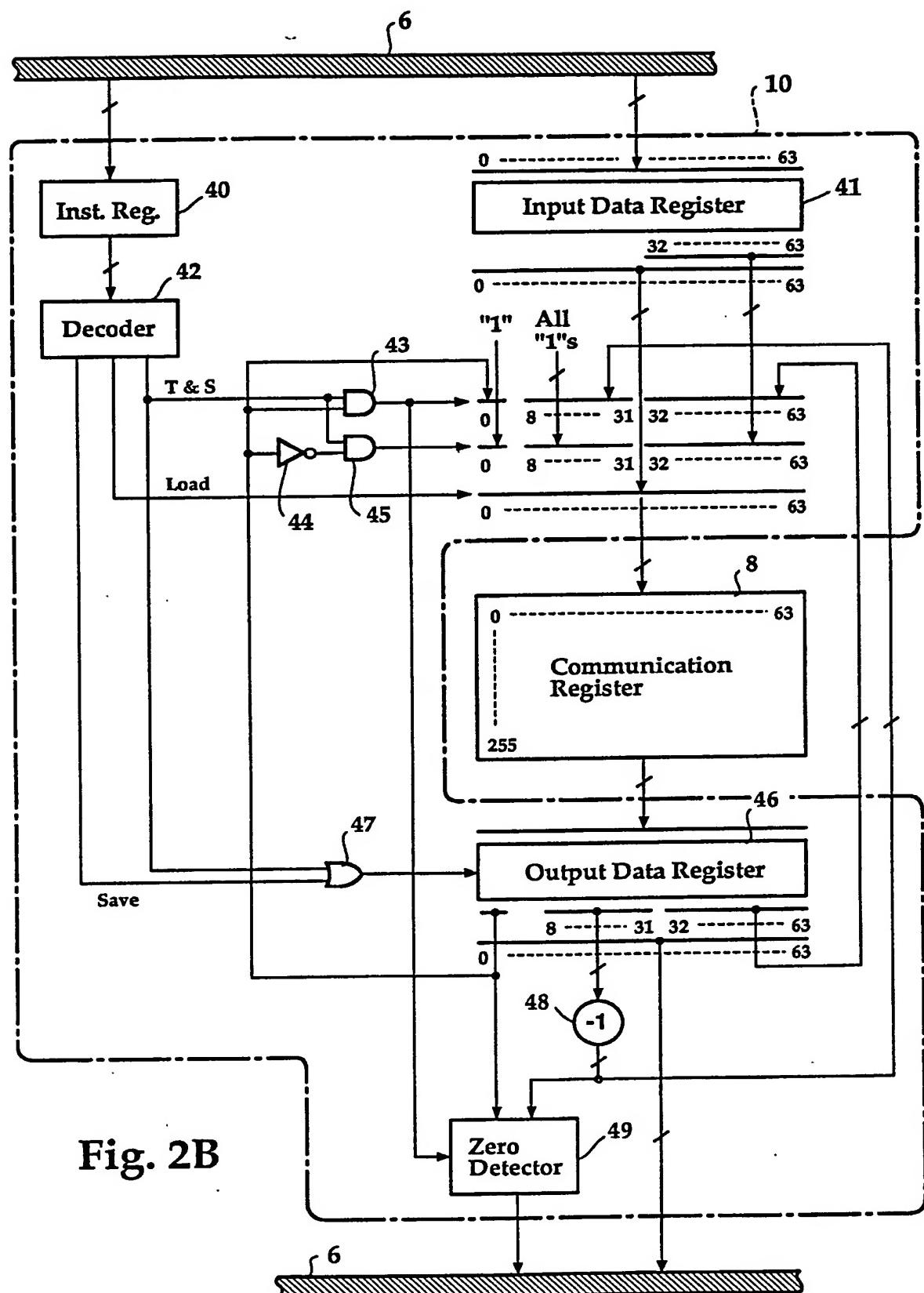
**Fig. 2B**

Fig. 4

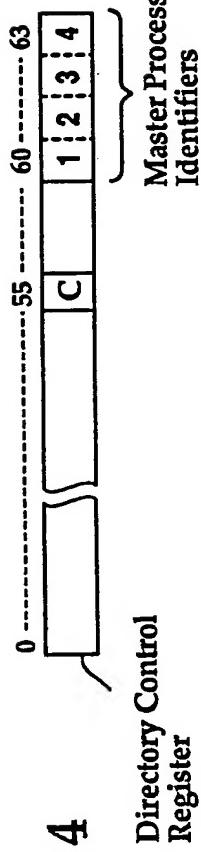


Fig. 6

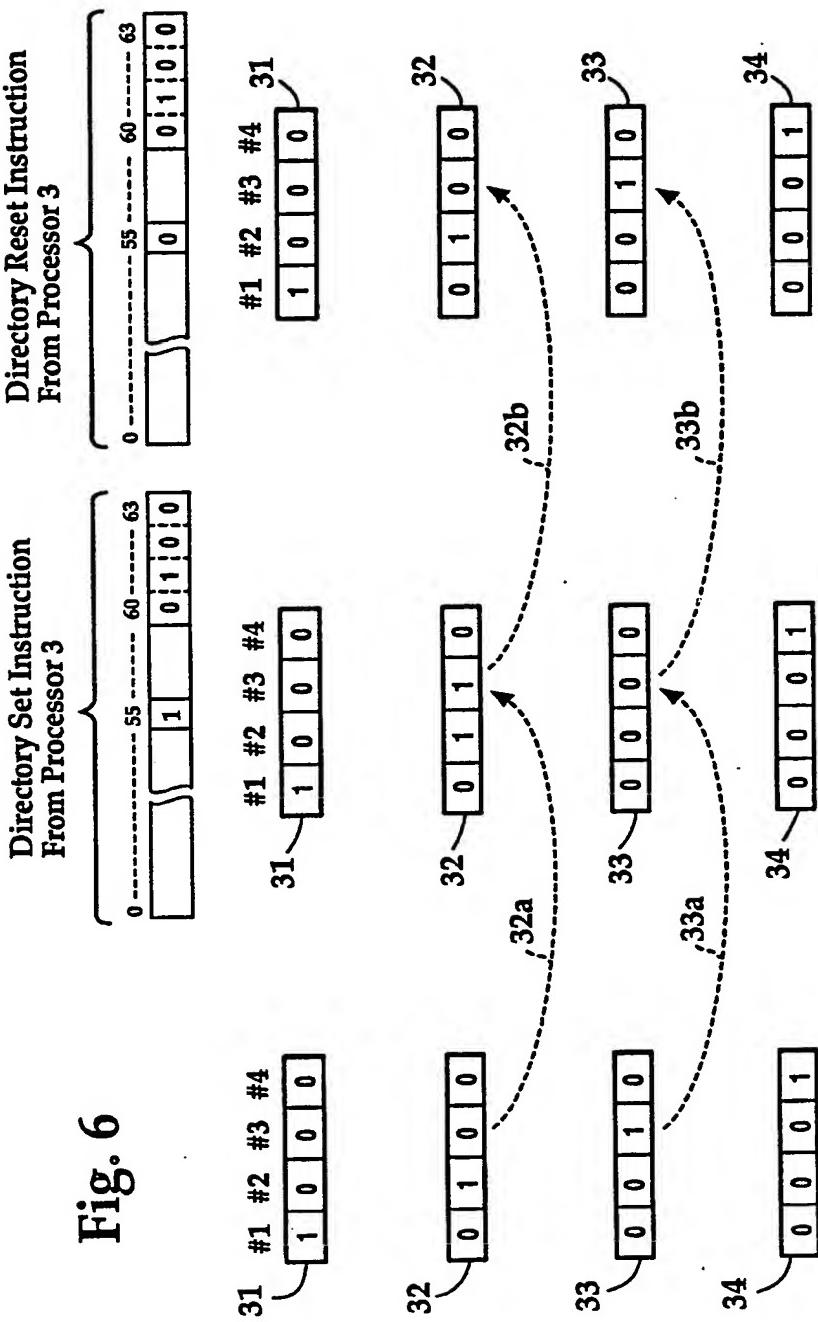


Fig. 5A

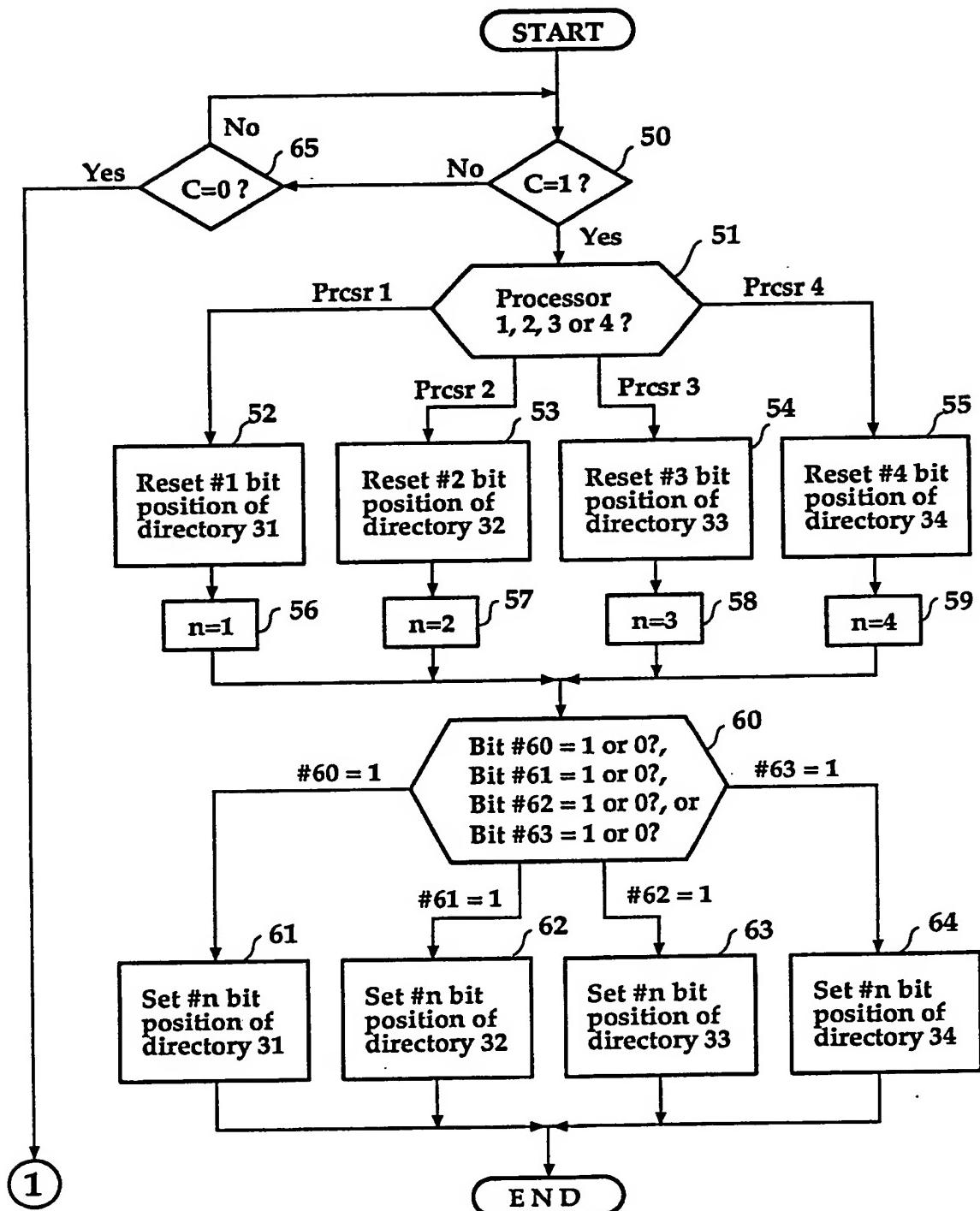
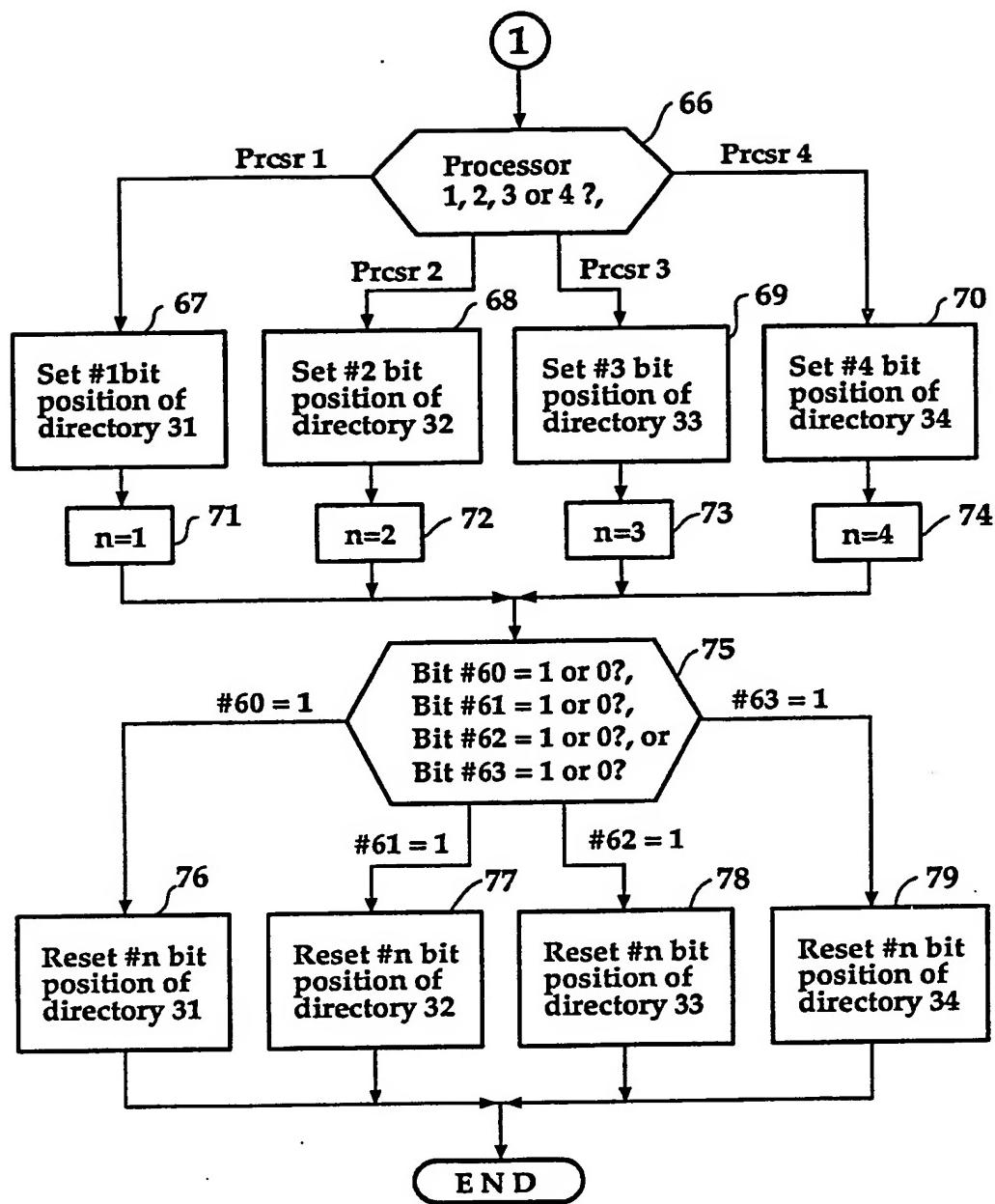


Fig. 5B





{19}



JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

(11) Publication number: 04070439 A
(43) Date of publication of application: 05.03.1992

(51) Int. Cl. E04B 1/24
E04C 3/32

(21) Application number: 02184827
(22) Date of filing: 11.07.1996

(54) PILLAR BODY FOR MOUNTING BEAM

(57) Abstract:

PURPOSE: To obviate the welding work in the site so as to enhance the working efficiency by protruding a bolt shaft to a pillar base body, formed of a short scale angle steel pipe, from the reverse side through a back board material and also screwing a beam mounting metal fixture thereafter fixing a beam.

CONSTITUTION: A plurality of bolt shafts 6 are protruded at a right angle to a pillar base body 2, consisting of a short scale angle steel pipe of sectional shape equal to a pillar body 1, from each surface in the reverse side through a back board material of width not interfering with each other. Next, a beam mounting member 32 is screwed to the pillar base body 2 by bolts 6 while fixing the pillar base body 2 to a beam mounting position of the pillar body 1. Further, a beam

(71) Applicant: NATL HOUSE IND CO LTD

(72) Inventor: YAMAOKA MASAKI

D is fixed by bolts to the beam mounting metal fixture
32. In a work spot, assembly is performed without performing welding work. In this way, efficiency of work can be improved.

COPYRIGHT: (C)1992.JPO&Japio

